

LISA-U1 series

3.75G UMTS/HSPA

Wireless Modules

Data Sheet

Abstract

Technical data sheet describing the LISA-U1 series UMTS/HSPA wireless modules.

These modules are a complete and cost efficient 3.75G solution offering high-speed dual-band HSDPA/HSUPA and quad-band GSM/GPRS voice and/or data transmission technology in a compact form factor.



33.2 x 22.4 x 2.7 mm

Document Information

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Document status information

Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	Firmware version	PCN / IN
LISA-U100	LISA-U100-00S-00	10.72	n.a.
LISA-U110	LISA-U110-00S-00	10.72	n.a.
LISA-U120	LISA-U120-00S-00	10.72	n.a.
LISA-U130	LISA-U130-00S-00	10.72	n.a.

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1 Functional description

1.1 Overview

LISA-U1 series modules are a 3.5G/3.75G solution providing full dual-band HSxPA and quad-band GSM/EDGE data and voice transmission in a compact form factor. These modules feature low power consumption, and GSM/E-GPRS class 12 data transmission with voice capability. They also combine baseband, RF transceiver, power management unit, and power amplifier in a single, easy-to-integrate solution.

LISA-U1 modules are complete, fully qualified and certified solutions, which reduces cost and enables short time to market. They are ideally suited to M2M and automotive applications such as: mobile Internet terminals and applications, car infotainment and telematics, Automatic Meter Reading (AMR), Remote Monitoring Automation and Control (RMAC), surveillance and security, eCall, road pricing, asset tracking, fleet management, anti theft systems, and Point of Sales (PoS) terminals.

LISA-U1 modules support full access to u-blox GPS receivers via serial port. Thus WCDMA/GSM and GPS can be controlled through a single serial port from any host processor. The compact LISA form factor and SMT pads allow fully automated assembly with standard pick & place and reflow soldering equipment for cost-efficient, high-volume production.

1.2 Product features

Module	Technology		Bands	Interface					Audio	Functions														
	HSUPA [Mb/s]	HSDPA [Mb/s]	UMTS/HSPA bands [MHz]	GSM/GPRS/EDGE quad-band	UART	SPI (5 wires)		USB	DDC for u-blox GPS	GPIO	Analog Audio	Digital Audio	Network indication	Antenna Supervisor	Jamming detection	Embedded TCP/UDP stack	FTP, HTTP	SSL	GPS via Modem	Embedded AssistNow Software	FW update over AT (FOAT)	FW update over the air (FOTA)	In-band modem	CellLocate
LISA-U100	5.76	7.2	850/1900	•	1	1	1	1	5				•	•	U	•	U	U	•	•	U	A	U	
LISA-U110	5.76	7.2	900/2100	•	1	1	1	1	5				•	•	U	•	U	U	•	•	U	A	U	
LISA-U120	5.76	7.2	850/1900	•	1	1	1	1	5	1	1		•	•	U	•	U	U	•	•	U	A	U	
LISA-U130	5.76	7.2	900/2100	•	1	1	1	1	5	1	1		•	•	U	•	U	U	•	•	U	A	A	U

A = available upon request

U = available in the next firmware version

Table 1: LISA-U1 series features

1.3 Block diagram

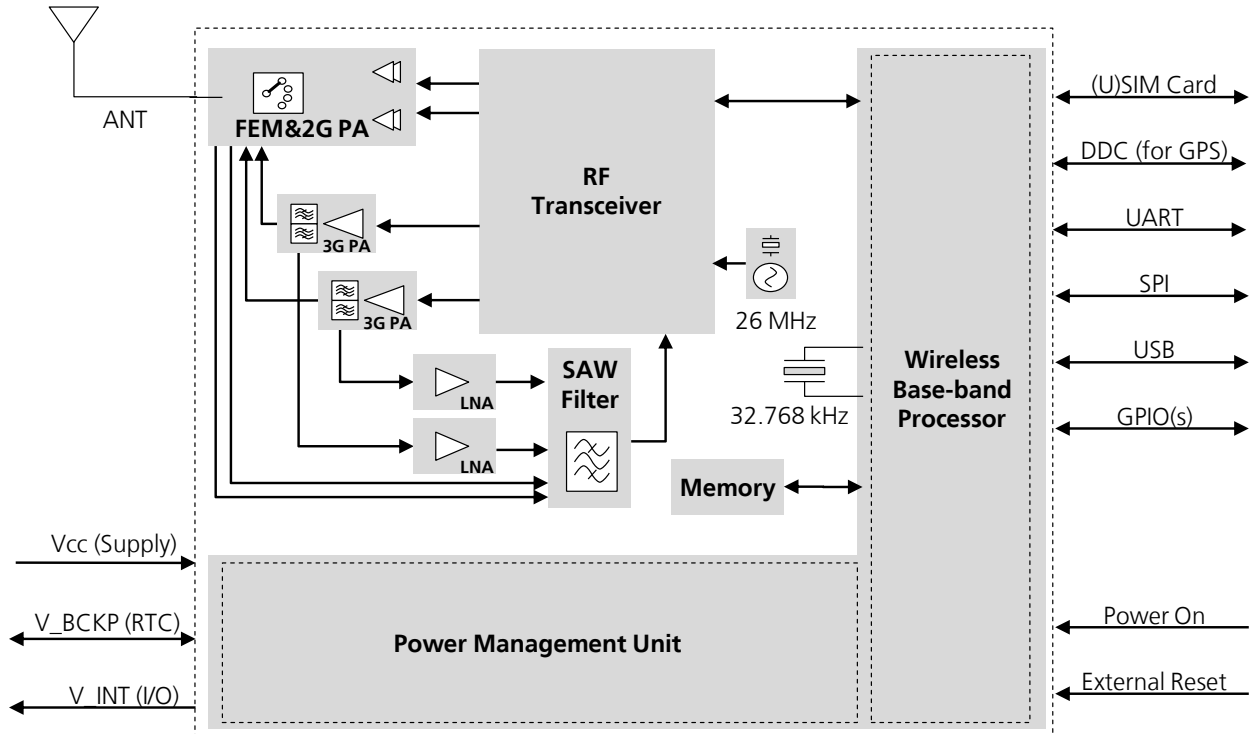


Figure 1: LISA-U100 / LISA-U110 block diagram

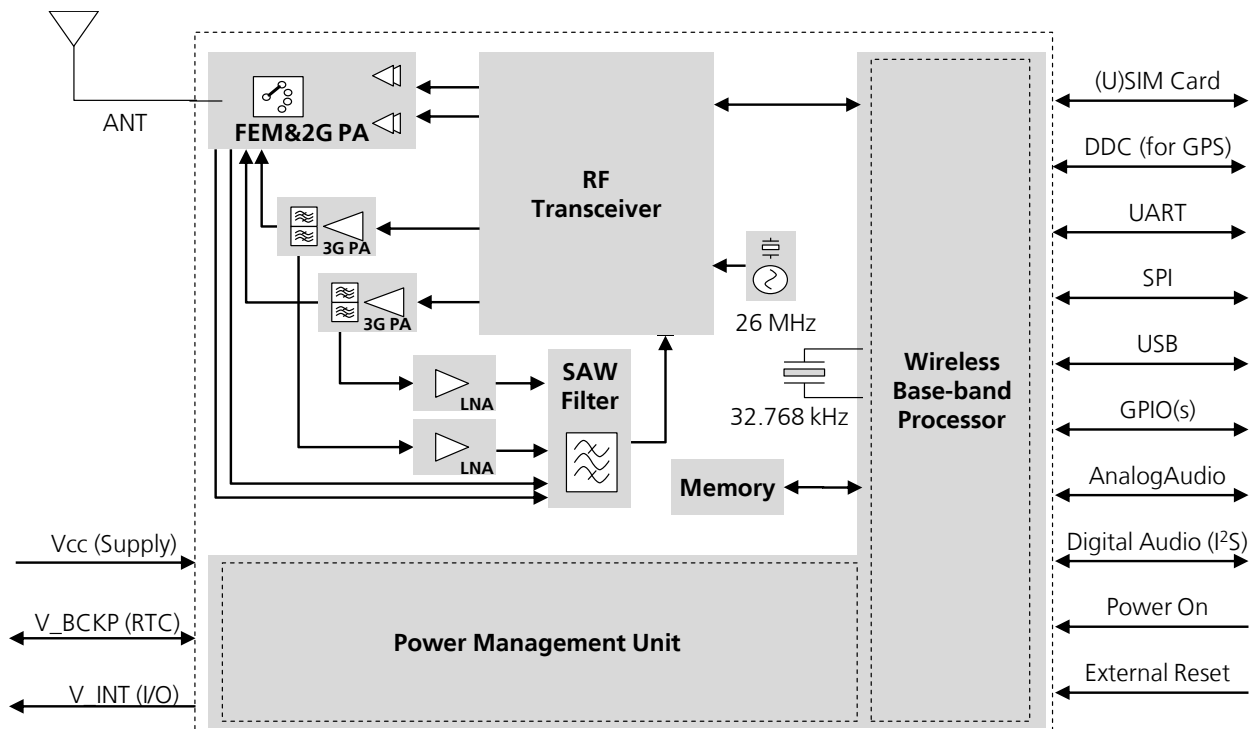


Figure 2: LISA-U120 / LISA-U130 block diagram

1.4 Product description

LISA-U1 wireless modules integrate full-feature 3G UMTS/HSxPA and 2G GSM/GPRS/EDGE protocol stack with Assisted GPS support. These SMT modules come in the compact LISA form factor, featuring Leadless Chip Carrier (LCC) packaging technology.

3G UMTS/HSDPA/HSUPA Characteristics	2G GSM/GPRS/EDGE Characteristics
Class A User Equipment ¹	Class B Mobile Station ²
UMTS Terrestrial Radio Access (UTRA) Frequency Division Duplex (FDD) operating mode	
Dual-band support: <ul style="list-style-type: none"> Band II (1900 MHz) and Band V (850 MHz) for LISA-U100, LISA-U120 Band I (2100 MHz) and Band VIII (900 MHz) for LISA-U110, LISA-U130 	Quad-band support <ul style="list-style-type: none"> GSM 850 MHz, E-GSM 900 MHz, DCS 1800 MHz and PCS 1900 MHz
WCDMA/HSDPA/HSUPA <ul style="list-style-type: none"> Power Class 3 (24 dBm) for WCDMA/HSDPA/HSUPA mode 	GSM/GPRS <ul style="list-style-type: none"> Power Class 4 (33 dBm) for GSM/E-GSM bands Power Class 1 (30 dBm) for DCS/PCS bands EDGE <ul style="list-style-type: none"> Power Class E2 (27 dBm) for GSM/E-GSM bands Power Class E2 (26 dBm) for DCS/PCS bands
PS <ul style="list-style-type: none"> HSUPA category 6, up to 7.2 Mb/s DL, 5.76 Mb/s UL HSDPA category 8, up to 7.2 Mb/s DL, 384 kb/s UL WCDMA PS data up to 384 kb/s DL/UL 	PS <ul style="list-style-type: none"> GPRS multislot class 12³, coding scheme CS1-CS4, up to 85.6 kb/s EDGE multislot class 12³, coding scheme MCS1-MCS9, up to 236.8 kb/s
WCDMA CS data up to 64 kb/s DL/UL	CS (Circuit Switched) Data calls are supported in transparent/non transparent mode up to 9.6 kb/s

Table 2: LISA-U1 UMTS/HSDPA/HSUPA and GSM/GPRS/EDGE characteristics

Operation modes I to III are supported on GSM/GPRS network, with user-defined preferred service selectable from GSM to GPRS. Paging messages for GSM calls can be monitored during GPRS data transfer in not-coordinating NOM II-III.

The network automatically configures the number of timeslots used for reception or transmission (voice calls take precedence over GPRS traffic) and channel encoding (CS1 to MCS9). The maximum (E)GPRS bit rate of the mobile station depends on the coding scheme and number of time slots. Direct Link mode is supported for TCP sockets.

¹ Device can work simultaneously in Packet Switch and Circuit Switch mode: voice calls are possible while the data connection is active without any interruption in service.

² Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time. If for example during data transmission an incoming call occurs, the data connection is suspended to allow the voice communication. Once the voice call has terminated, the data service is resumed.

³ GPRS/EDGE multislot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total. GPRS class determines the number of timeslots available for upload and download and thus the speed at which data can be transmitted and received, with higher classes typically allowing faster data transfer rates.

Basic features ⁴	Supplementary services	Short Message Service (SMS)
Display of Called Number	Call Hold/Resume (CH)	SMS Classes 1, 2, 3
Indication of Call Progress Signals	Call Waiting (CW)	Mobile-Originating SMS (MO SMS)
Country/PLMN Indication	Multi-Party (MTPY)	Mobile-Terminating SMS (MT SMS)
International Access Function	Call Forwarding (CF)	SMS Cell Broadcast (SMS CB)
Service Indicator	Call Divert	Text and PDU mode supported
Dual Tone Multi Frequency (DTMF)	Explicit Call Transfer (ECT)	SMS during circuit-switched calls
Subscription Identity Management	Call Barring (CB)	SMS over PSD or CSD
Service Provider Indication	Call Completion to Busy Subscriber (CCBS)	SMS storage on SIM and memory module
Abbreviated Dialing	Advice of Charge Charging (AOCC)	
SIM Toolkit	Calling Line Identification Presentation (CLIP)	
	Calling Line Identification Restriction (CLIR)	
	Connected Line Identification Presentation (COLP)	
	Connected Line Identification Restriction (COLR)	
	Unstructured Supplementary Services Data (USSD)	
	Network Identify and Time Zone (NITZ)	

Table 3: Basic Features⁴, Supplementary Services, and Short Message Service (SMS)

1.5 AT Command support

The module supports AT commands according to 3GPP standards: TS 27.007 [1], 27.005 [2], 27.010 [3], and the u-blox AT command extension.



For the complete list of the supported AT commands and their syntax see the u-blox AT Commands Manual [5].

1.6 AssistNow clients and GPS integration

For customers using u-blox GPS receivers, LISA-U1 series modules feature embedded AssistNow Online and AssistNow Offline clients. AssistNow A-GPS provides better GPS performance and faster Time-To-First-Fix. The clients can be enabled / disabled with an AT command.

LISA-U1 series modules act as a stand-alone AssistNow client, making AssistNow available with no additional requirements for resources or software integration on an external host micro controller. Full access to u-blox GPS receivers is available via the LISA-U1 series, through a dedicated DDC (I²C) interface. This means that GSM/WCDMA and GPS can be controlled through a single serial port from any host processor.

For more details, see the GPS Implementation in wireless modules Application Note [7].

⁴ These functionalities are supported via AT commands (for more details see the u-blox AT Commands Manual [5]).

1.7 In-Band modem (LISA-U130 only)



The feature will be available in the next firmware version.

LISA-U130 supports In-Band modem for eCall, according to the 3GPP TS 26.267 specification [9].

According to the eCall (Pan-European automatic in-vehicle emergency call system) specification, an eCall must be generated automatically or manually following a car accident, using GSM cellular service “112”. When activated, the in-vehicle eCall system (IVS) creates an emergency call carrying both voice and data (e.g. vehicle GPS position) directly to the nearest 112 Public Safety Answering Point (PSAP).

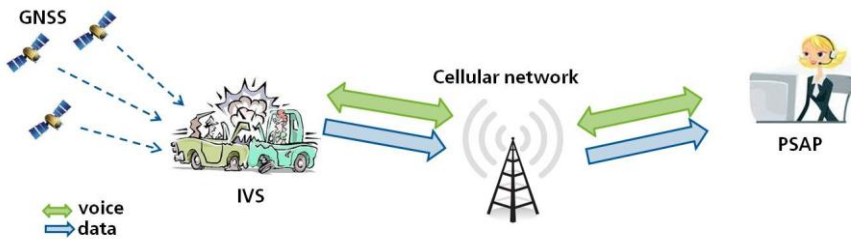


Figure 3: In-Band modem diagram flow

In-band modem enables transmission of vehicle Minimum Set of Data (MSD - 140 bytes) and the establishment of a voice emergency call using the same physical channel (voice channel) without any modifications of the existing cellular network architecture.

In-Band modem is a mandatory feature to meet the eCall requirements and to develop in vehicle devices fully supporting eCall.

The in-Band modem functionality is delivered upon request.

1.8 Smart temperature supervision

An internal sensor is used to constantly monitor the temperature of LISA-U1 series modules. The measured temperature is compared with the internally predefined thresholds .

LISA module gives a warning when the measured temperature is inside the valid range (i.e. the module is still in a valid and good working condition) but it is close to the limit (upper or lower limits).

Thermal shutdown is notified and automatically forced by the module when the temperature value is outside the specified range (i.e. the module is in a dangerous working condition). For security reasons the shutdown is suspended in case of emergency call in progress: in this case the device will switch off at call termination.

Smart Temperature Supervisor feature can be enabled or disabled via an AT command (for more details please to u-blox AT commands manual [5], +USTS AT command). If the feature is disabled there is no embedded protection against not allowed temperature working conditions.



The sensor measures the board temperature inside the shields, which can differ from ambient temperature.

2 Interfaces

2.1 Power Management

2.1.1 Module supply (VCC)

LISA-U1 series modules must be supplied through the **VCC** pin by a DC power supply. Voltages must be stable: during operation, the current drawn from **VCC** can vary by some order of magnitude, especially due to the surging consumption profile of the GSM system (described in the LISA-U1 series System Integration Manual [6]). It is important that the system power supply circuit is able to support peak power.

2.1.2 RTC supply (V_BCKP)

V_BCKP is the Real Time Clock (RTC) supply. When VCC voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the RTC and the same supply voltage will be available on **V_BCKP** pin. If the VCC voltage is under the minimum operating limit (e.g. during not powered mode), the RTC can be externally supplied via **V_BCKP** pin.

2.1.3 Digital I/O interfaces supply (V_INT)

LISA-U1 series modules provide an internally generated supply rail output for digital interfaces (**V_INT**). This can be used in place of an external discrete regulator to supply pull-up resistors on the DDC interface. This optimizes the bill of material for various applications, e.g. with u-blox GPS operating at 1.8 V.

2.2 RF antenna interface

The **ANT** pad has an impedance of 50 Ω and provides the RF antenna interface.

2.3 System functions

2.3.1 Module power-on (PWR_ON)

- By shorting the **PWR_ON** pin to ground: the **PWR_ON** pin requires an external pull-up resistor to set its value to logic high and must not be left floating. Internal circuitry is sensitive to a falling edge
- By a rising edge on the **VCC** pin to a valid voltage as module supply, by a preset RTC alarm and by a rising edge on the **RESET_N** pin

2.3.2 External reset (RESET_N)

- **RESET_N** pin must be shorted to ground. Driving **RESET_N** pin low causes an asynchronous “external” or “hardware” reset of the entire module, including the integrated power management unit, except for the RTC internal block: the **V_INT** interfaces supply is switched off and all the digital pins are tri-stated, but the **V_BCKP** supply and the RTC block are enabled
- With AT+CFUN command (more details in u-blox AT Commands Manual [5]). An “internal” or “software” reset is performed, causing an asynchronous reset of the baseband processor, excluding the integrated

power management unit and the RTC internal block: the **V_INT** interfaces supply is enabled and each digital pin is set in its internal reset state, the **V_BCKP** supply and the RTC block are enabled

2.4 (U)SIM interface

A (U)SIM card interface is provided on the SMT pads of the LISA-U1 series modules: the high-speed SIM/ME interface is implemented as well as automatic detection of the required SIM supporting voltage.

Both 1.8 V and 3 V SIM types are supported (1.8 V and 3 V ME). Activation and deactivation with automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values proposed by the SIM Card.

2.5 Serial communication

LISA-U1 series modules provide the following serial communication interfaces where AT command interface and Packet-Switched / Circuit-Switched Data communication are concurrently available:

- One asynchronous serial interface (UART)
- One Inter Processor Communication (IPC) interface that includes a synchronous SPI-compatible interface
- One high-speed USB 2.0 compliant interface

The following serial communication interfaces can be used for firmware upgrade:

- The UART interface, using the **RxD** and **TxD** lines only
- The USB interface, using all the provided lines (**VUSB_DET**, **USB_D+** and **USB_D-**)

2.5.1 Asynchronous serial interface (UART)

The UART interface is a 9-wire unbalanced asynchronous serial interface provided for all communications with LISA-U1 series modules.

UART features are:

- Complete serial port with RS-232 functionality conforming to the ITU-T V.24 Recommendation [4], with CMOS compatible signal levels (0 V for low data bit or ON state and 1.8 V for high data bit or OFF state)
- Data lines (**RxD** as output, **TxD** as input), hardware flow control lines (**CTS** as output, **RTS** as input), modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output) are provided
- Hardware flow control (default value), software flow control, or none flow control are supported
- Power saving indication available⁵ on the hardware flow control output (**CTS** line): the line is driven to the OFF state when the module is not prepared to accept data by the UART interface
- 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400 and 460800 b/s baud rates are supported for the AT interface
- Default baud rate is 115200 b/s
- Autobauding is not supported
- Frame format can be:
 - 8N2 (8 data bits, no parity, 2 stop bits)
 - 8N1 (8 data bits, no parity, 1 stop bit)

⁵ If enabled

- 8E1 (8 data bits, even parity, 1 stop bit)
- 8O1 (8 data bits, odd parity, 1 stop bit)
- 7E1 (7 data bits, even parity, 1 stop bit)
- 7O1 (7 data bits, odd parity, 1 stop bit)
- Default frame configuration is 8N1

UART serial interface can be opportunely configured through AT commands. For more details please refer to u-blox AT Commands Manual [5] (+IPR, +ICF, +IFC, &K, \Q, +UPSV AT command) and LISA-U1 series System Integration Manual [6].

2.5.2 Universal Serial Bus (USB)

The LISA-U1 series modules include a high-speed USB 2.0 compliant interface with maximum throughput of 480 Mb/s. The module itself acts as a USB device and can be connected to any USB host.

The USB is the main interface for transferring high speed data between LISA-U1 series and a host processor.

Signals **USB_D+/USB_D-** carry the USB serial data and signaling. The USB interface is automatically enabled by a valid USB VBUS supply voltage (5.0 V typical) on **VUSB_DET** pin.

The module simultaneously provides 6 USB CDCs (Communications Device Class) with this configuration:

- USB1: AT commands / data connection
- USB2: AT commands / data connection
- USB3: AT commands / data connection
- USB4: GPS tunneling dedicated port
- USB5: 2G trace dedicated port (debug purpose)
- USB6: 3G trace dedicated port (debug purpose)

The user can concurrently use AT command interface on one CDC and Packet-Switched / Circuit-Switched Data communication on another CDC.

2.5.3 Serial Peripheral Interface (SPI)

The LISA-U1 series modules include a synchronous SPI-compatible serial interface. The LISA-U1 series run natively as an SPI slave.

The LISA-U1 series modules provide two handshake signals (**SPI_MRDY** and **SPI_SRDY**), added to the standard 3-wire SPI serial interface (**SPI_MOSI**, **SPI_MISO**, **SPI_SCLK**), implementing the 5-wire Inter Processor Communication (IPC) interface.

The SPI / IPC interface can be used for high speed data transfer (UMTS/HSPA) between LISA-U1 series modules and the host processor. The high speed communication (up to 26 Mb/s) between the two processors is possible only if both sides follow the same Inter Processor Communication (IPC) specifications.

Refer to LISA-U1 series System Integration Manual [6] and SPI Interface Application Note [12] for a detailed description of the implementation of the SPI / IPC protocol.

2.5.4 Mux protocol

The LISA-U1 series module has a software layer with MUX functionality, 3GPP TS 27.010 Multiplexer Protocol [3], available either on the UART or on the SPI physical link.



The USB interface does not support the multiplexer protocol TS 27.010.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows simultaneous sessions over the used physical link (UART or SPI): the user can concurrently use AT command interface on one MUX channel and Packet-Switched / Circuit-Switched Data communication on another MUX channel. The multiplexer protocol can be used on one serial interface (UART or SPI) at a time. Each session consists of a stream of bytes transferring various kinds of data such as SMS, CBS, PSD, GPS, AT commands in general.

The following channels are defined:

- Channel 0: control channel
- Channel 1 – 5: AT commands / data connection
- Channel 6: GPS tunneling

This permits, for example, an SMS to be transferred to the DTE when a data connection is in progress.

For more details please refer to the GSM MUX Implementation Application Note [8].

2.6 DDC (I²C) bus interface

The LISA-U1 series modules include an I²C compatible DDC interface exclusively for communication with u-blox GPS devices.

2.7 Audio (LISA-U120 / U130 only)

The LISA-U120 / U130 modules provide one analog and one digital audio interface:

- Analog audio interface: a differential analog microphone⁶ input (**MIC_P/MIC_N**) shared for all uplink analog path modes (handset, headset and hands-free) and a differential analog output (**SPK_P/SPK_N**) shared for all downlink analog path modes (earpiece, headset and loudspeaker). The uplink or downlink analog path profiles use the same physical input or output but have different sets of audio parameters (for more details please refer to u-blox AT Commands Manual [5], AT+USPM, AT+USGC, AT+UDBF, AT+USTN commands)
- Digital audio interface: a 4-wire I²S digital audio interface, including **I2S_CLK**, **I2S_RXD**, **I2S_TXD**, **I2S_WA**. This audio path is selected when parameters <main_uplink> and <main_downlink> in AT+USPM command (for more details please refer to u-blox AT Commands Manual [5]) are respectively "I²S input line" and "I²S output line"

For further details about the hardware integration of the audio interface in an application design, refer to the LISA-U1 series System Integration Manual [6].

For further details about the possible settings of the audio interface, as well as the allowed input/output audio path combinations and as the default values related to the uplink/downlink path, refer to u-blox AT Commands Manual [5], +USPM AT command.

2.8 GPIO

The LISA-U1 series modules provide 5 pins (**GPIO1**, **GPIO2**, **GPIO3**, **GPIO4** and **GPIO5**) which can be configured as a general purpose input or output, or can be configured to provide special functions via u-blox AT commands (for further details please refer to the LISA-U1 series System Integration Manual [6] and refer to the u-blox AT Commands Manual [5], +UGPIOC, +UGPIOR, +UGPIOW, +UGPS, +UGPRF).

The following functions are available in the LISA-U1 series modules:

- **GSM Tx burst indication:** the **GPIO1** pin can be configured to indicate when a GSM transmit slot occurs

⁶ On LISA-U1 series the microphone supply is not available

- **GPS supply enable:** the **GPIO2** pin is by default configured to enable or disable the supply of the u-blox GPS receiver connected to the LISA-U1 series module
- **SIM card detection:** the **GPIO5** pin is by default configured to sense SIM card presence
- **Network status indication:** each GPIO can be configured to indicate network status (registered home network, registered roaming, data transmission, no service)
- **General purpose input:** all the 5 GPIOs can be configured as input, sensing high or low digital level
- **General purpose output:** all the 5 GPIOs can be configured as output, set in the high or low digital level
- **Pad disabled:** all the 5 GPIOs can be configured in tri-state, with an internal active pull-down enabled. The **GPIO1, GPIO3, GPIO4** pins are by default configured as “pad disabled” (not used mode)



The following functions will be available in the next firmware version of LISA-U1 series modules:

- **GPS data ready:** the **GPIO3** pin by default configured to sense when the u-blox GPS receiver connected to the LISA-U1 series module is ready to send data by the DDC (I²C) interface
- **GPS RTC sharing:** the **GPIO4** pin by default configured to provide a RTC (Real Time Clock) synchronization signal to the u-blox GPS receiver connected to the LISA-U1 series module

3 Pin definition

3.1 Pin assignment



Figure 4: LISA-U1 series pin assignment

No	Module	Name	Power domain	I/O	Description	Remarks
1	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
2	All	V_BCKP	-	I/O	Real Time Clock supply input/output	V_BCKP = 2.3 V (typical) generated by the module to supply the Real Time Clock when VCC supply voltage is within valid operating range. A backup battery can be connected to this pin to supply the Real Time Clock when VCC supply voltage is not within valid operating range. See section 4.2.3 for detailed electrical specs.
3	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
4	All	V_INT	-	O	Digital I/O Interfaces supply output	V_INT = 1.8V (typical) generated by the module when it is switched-on and the RESET_N (external reset input pin) is not forced to the low level. See section 4.2.3 for detailed electrical specs.
5	All	RSVD	-	N/A	RESERVED pin	This pin has special function: it must be connected to GND to allow module to work properly.

No	Module	Name	Power domain	I/O	Description	Remarks
6	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
7	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
8	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
9	All	DSR	GDI	O	UART data set ready	Circuit 107 (DSR) in ITU-T V.24. Output driver class B. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
10	All	RI	GDI	O	UART ring indicator	Circuit 125 (RI) in ITU-T V.24. Output driver class B. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
11	All	DCD	GDI	O	UART data carrier detect	Circuit 109 (DCD) in ITU-T V.24. Output driver class B. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
12	All	DTR	GDI	I	UART data terminal ready	Circuit 108/2 (DTR) in ITU-T V. 24. Internal active pull-up to V_INT enabled. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
13	All	RTS	GDI	I	UART ready to send	Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to V_INT enabled. PU/PD class c. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
14	All	CTS	GDI	O	UART clear to send	Circuit 106 (CTS) in ITU-T V.24. Output driver class B. PU/PD class c. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
15	All	TXD	GDI	I	UART transmitted data	Circuit 103 (TxD) in ITU-T V.24. Internal active pull-up to V_INT enabled. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
16	All	RXD	GDI	O	UART received data	Circuit 104 (RxD) in ITU-T V.24. Output driver class B. PU/PD class c. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
17	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
18	All	VUSB_DET	USB	I	USB detect input	Input for VBUS (5 V typical) USB supply sense. See section 4.2.10 for detailed electrical specs.
19	All	PWR_ON	POS	I	Power-on input	The PWR_ON pin has high input impedance: do not leave it floating in noisy environment (an external pull-up resistor is required) See section 4.2.6 for detailed electrical specs.
20	All	GPIO1	GDI	I/O	GPIO	Output driver class D. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
21	All	GPIO2	GDI	I/O	GPIO	Output driver class B. PU/PD class c. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
22	All	RESET_N	ERS	I	External reset input	Internal 10 kΩ pull-up resistor to V_BCKP. See section 4.2.7 for detailed electrical specs.
23	All	GPIO3	GDI	I/O	GPIO	Output driver class C_0. PU/PD class b_0. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
24	All	GPIO4	GDI	I/O	GPIO	Output driver class C_0. PU/PD class b_0. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
25	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
26	All	USB_D-	USB	I/O	USB Data Line D-	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [10] are part of the USB pad driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
27	All	USB_D+	USB	I/O	USB Data Line D+	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [10] are part of the USB pad driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
28	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
29	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
30	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
31	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
32	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
33	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
34	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
35	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
36	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
37	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
38	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
39	LISA-U100 / LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 / LISA-U130	MIC_N	AUDIO	I	Differential analog audio input (negative)	Differential analog input shared for all path modes: handset, headset, hands-free mode. Internal DC blocking capacitor. See section 4.2.12 for detailed electrical specs.
40	LISA-U100 / LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 / LISA-U130	MIC_P	AUDIO	I	Differential analog audio input (positive)	Differential analog input shared for all path modes: handset, headset, hands-free mode. Internal DC blocking capacitor. See section 4.2.12 for detailed electrical specs.
41	LISA-U100 / LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 / LISA-U130	I2S_WA	GDI	O	I ² S word alignment	Output driver class C. PU/PD class b. Value at internal reset: T/TPD. See section 4.2.9 for detailed electrical specs.
42	LISA-U100 / LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 / LISA-U130	I2S_TXD	GDI	O	I ² S transmit data	Output driver class C. PU/PD class b. Value at internal reset: T/TPD. See section 4.2.9 for detailed electrical specs.
43	LISA-U100 / LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U120 / LISA-U130	I2S_CLK	GDI	O	I ² S clock	Output driver class C. PU/PD class b. Value at internal reset: T/TPD. See section 4.2.9 for detailed electrical specs.
44	LISA-U100 / LISA-U110	RSVD	-	N/A	RESERVED pin	Leave unconnected.

No	Module	Name	Power domain	I/O	Description	Remarks
	LISA-U120 / LISA-U130	I2S_RXD	GDI	I	I ² S receive data	Internal active pull-up to V _{INT} enabled. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
45	All	SCL	DDC	O	I ² C bus clock line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
46	All	SDA	DDC	I/O	I ² C bus data line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
47	All	SIM_CLK	SIM	O	SIM clock	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
48	All	SIM_IO	SIM	I/O	SIM data	Internal 4.7 k Ω pull-up resistor to VSIM. Value at internal reset: L/PD. See section 4.2.8 for detailed electrical specs.
49	All	SIM_RST	SIM	O	SIM reset	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
50	All	VSIM	-	O	SIM supply output	VSIM = 1.80 V typical or 2.90 V typical generated by the module according to the SIM card type. See section 4.2.3 for detailed electrical specs.
51	All	GPIO5	GDI	I/O	GPIO	Output driver class A. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
52	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
53	LISA-U100 / LISA-U110 LISA-U120 / LISA-U130	RSVD SPK_P	- AUDIO	N/A O	RESERVED pin Differential analog audio output (positive)	Leave unconnected. Differential analog audio output shared for all path modes: earpiece, headset and loudspeaker mode. See section 4.2.12 for detailed electrical specs.
54	LISA-U100 / LISA-U110 LISA-U120 / LISA-U130	RSVD SPK_N	- AUDIO	N/A O	RESERVED pin Differential analog audio output (negative)	Leave unconnected. Differential analog audio output shared for all path modes: earpiece, headset and loudspeaker mode. See section 4.2.12 for detailed electrical specs.
55	All	SPI_SCLK	GDI	I	SPI Serial Clock. Master Output, Slave Input	Idle low (CPOL=0). Internal active pull-down to GND enabled. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
56	All	SPI_MOSI	GDI	I	SPI Data Line. Master Output, Slave Input	Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). Idle high. Internal active pull-up to V _{INT} enabled. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
57	All	SPI_MISO	GDI	O	SPI Data Line. Master Input, Slave Output	Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). Idle high. Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
58	All	SPI_SRDY	GDI	O	SPI Slave Ready to receive control line. Master Input, Slave Output	Idle low. Output driver class B. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
59	All	SPI_MRDY	GDI	I	SPI Master Ready to transmit control line. Master Output, Slave Input	Idle low. Internal active pull-down to GND enabled. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
60	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
61	All	VCC	-	I	Module supply input	All VCC pads must be connected to external supply
62	All	VCC	-	I	Module supply input	All VCC pads must be connected to external supply
63	All	VCC	-	I	Module supply input	All VCC pads must be connected to external supply
64	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
65	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
66	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
67	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
68	All	ANT	-	I/O	RF antenna	50 Ω nominal impedance
69	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
70	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
71	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
72	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
73	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
74	All	RSVD	-	N/A	RESERVED pin	Leave unconnected.
75	All	GND	-	N/A	Ground	All GND pads must be connected to ground.
76	All	GND	-	N/A	Ground	All GND pads must be connected to ground.

Table 4: Pinout


For more information about pinout see LISA-U1 series System Integration Manual [6].

See Appendix A for explanation of abbreviations and terms used.

4 Electrical specifications

Stressing the device above one or more of the ratings listed in the Absolute Maximum Rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating Conditions sections (chapter 4.2) of the specification should be avoided. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating conditions ranges define those limits within which the functionality of the device is guaranteed.
 Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum rating

Limiting values given below are in accordance with the Absolute Maximum Rating System (IEC 134).

Symbol	Description	Condition	Min.	Max.	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	-0.30	4.70	V
ICC	Module supply current	Input DC current at VCC pin		2.50	A
VUSB_DET	USB detection pin	Input DC voltage at VUSB_DET	-0.30	5.35	V
USB	USB D+/D- pins	Input DC voltage at USB_D+ and USB_D-	-1.00	5.35	V
V_BCKP	RTC supply voltage	Input DC voltage at V_BCKP pin	-0.15	2.50	V
GDI	Generic digital interfaces	Input DC voltage at Generic digital interfaces pins	-0.30	3.60	V
DDC	DDC interface	Input DC voltage at DDC interface pins	-0.30	3.60	V
SIM	SIM interface	Input DC voltage at SIM interface pin	-0.30	3.60	V
ERS	External reset signal	Input DC voltage at External reset signal pin	-0.15	2.50	V
POS	Power-on input	Input DC voltage at Power-on signal pin	-0.30	4.70	V
AUDIO	Audio input pins	Input DC voltage at Audio pins	-0.15	3.00	V
V_ANT	Antenna voltage	Input DC voltage at ANT pin	-0.15	3.00	V
P_ANT	Antenna power	Input RF power at ANT pin		10	dBm
Rho_ANT	Antenna ruggedness	Output RF load mismatch ruggedness at ANT pin		10:1	VSWR
Tstg	Storage Temperature		-40	85	°C

Table 5: Absolute maximum ratings

The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD

Parameter	Min.	Typ.	Max.	Unit	Remarks
ESD sensitivity for all pins except ANT pin			1000	V	Human Body Model according to JESD22-A114F
ESD immunity for ANT pin			500	V	According to IEC 61000-4-2

Table 6: Maximum ESD ratings

 **LISA-U1 series modules are Electrostatic Sensitive Devices (ESD) and require special precautions when handling.**

4.2 Operating conditions



Unless otherwise indicated, all operating condition specifications are at an ambient temperature of 25°C.



Operation beyond the operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating temperature range

Symbol	Parameter	Min.	Typ.	Max.	Units	Remarks
Topr	Operating temperature range	-40		+85	°C	
		-20		+65	°C	Normal operating temperature range See chapter 4.2.1.1
		-40		-20	°C	Extended operating temperature range 1 See chapter 4.2.1.2
		+65		+85	°C	Extended operating temperature range 2 See chapter 4.2.1.3

Table 7: Environmental conditions

4.2.1.1 Normal operating temperature range

The wireless module is fully functional and meets the ETSI specification across the specified temperature range.

4.2.1.2 Extended operating temperature range 1

The wireless module is fully functional across the specified temperature range. Occasional deviations from the ETSI specification may occur.

4.2.1.3 Extended operating temperature range 2

The wireless module is functional across the specified temperature range. Occasional deviations from the ETSI specification may occur. Thermal protection including automatic shutdown is implemented. Thermal protection is disabled for emergency calls. For more details, please refer to u-blox AT Commands Manual [5], +USTS AT command).

4.2.2 Module-to-Ambient thermal resistance

Symbol	Parameter	Module	Min.	Typ.	Max.	Units	Remarks
R _{th,M-A}	Module-to-Ambient thermal resistance	All	9		12	°C/W	Module mounted on a PCB with a high coverage of copper in still air conditions
R _{th,M-C}	Module internal-to-Case thermal resistance	All	1.5		3.5	°C/W	Referred to temperature difference between internal temperature sensor and module application baseboard, held at ambient temperature by thermal heat-sink and forced air ventilation.

Table 8: Module-to-Ambient thermal resistance

4.2.3 Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Module supply input voltage	3.40	3.80	4.20	V
ICC_PEAK	Module supply peak current consumption: peak of current consumption through the VCC pad during a GSM transmit burst, at VCC = 3.8 V, with a matched antenna (typ. value) or with a mismatched antenna (max. value) ⁷		2.00	2.50	A
V_BCKP	RTC supply input voltage	1.00	2.30	2.50	V
I_BCKP	RTC supply average current consumption, at V_BCKP = 2.3 V		2.50		μA

Table 9: Input characteristics of Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VSIM	SIM supply output voltage	1.76	1.80	1.83	V
		2.84	2.90	2.94	V
V_BCKP	RTC supply output voltage	2.19	2.30	2.42	V
I_BCKP	RTC supply output current capability			3	mA
V_INT	Digital I/O Interfaces supply output voltage	1.76	1.80	1.85	V
I_INT	Digital I/O Interfaces supply output current capability			50	mA

Table 10: Output characteristics of Supply/Power pins

⁷ Use this figure to dimension maximum current capability of power supply.

4.2.4 Power consumption

Table 11 reports power consumption of LISA-U1 series module⁸.

Mode	Condition	Power Consumption ⁹
Power Off Mode	Module is switched off	< 90 μ A
GSM/GPRS/EDGE Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV)	GSM 850 / E-GSM 900 / DCS 1800 / PCS 1900 bands DRX = 5 ¹⁰ USB interface not attached to a USB host	< 2 mA
	GSM 850 / E-GSM 900 / DCS 1800 / PCS 1900 bands DRX = 5 ¹⁰ USB interface in the suspend state	< 2.5 mA
GSM Talk (Connected) Mode	GSM 850 / E-GSM 900 bands Maximum Tx power (32.5 dBm typ.)	< 250 mA
	DCS 1800 / PCS 1900 bands Maximum Tx power (29.5 dBm typ.)	< 200 mA
GPRS TBF (Connected) Mode	GSM 850 / E-GSM 900 bands 4 Tx +1 Rx slots (up to 85.6 kb/s UL, 21.4 kb/s DL) Maximum Tx power (31.0 dBm typ.)	< 660 mA
	DCS 1800 / PCS 1900 bands 4 Tx +1 Rx slots (up to 85.6 kb/s UL, 21.4 kb/s DL) Maximum Tx power (28.0 dBm typ.)	< 440 mA
EDGE TBF (Connected) Mode	GSM 850 / E-GSM 900 bands 4 Tx +1 Rx slots (up to 236.8 kb/s UL, 59.2 kb/s DL) Maximum Tx power (25.0 dBm typ.)	< 460 mA
	DCS 1800 / PCS 1900 bands 4 Tx +1 Rx slots (up to 236.8 kb/s UL, 59.2 kb/s DL) Maximum Tx power (24.0 dBm typ.)	< 340 mA
UMTS/HSxPA Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV)	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 DRX = 7 ¹¹ USB interface not attached to a USB host	< 2 mA
	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 DRX = 7 ¹¹ USB interface in the suspend state	< 2.5 mA
UMTS Talk (Connected) Mode	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 12.2 kb/s UL, 12.2 kb/s DL Maximum Tx power (23.0 dBm typ.)	< 620 mA
HSDPA (Connected) Mode	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 Maximum Tx power (23.0 dBm typ.)	< 670 mA
HSUPA (Connected) Mode	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 5.76 Mb/s UL, 384 kb/s DL Maximum Tx power (21.5 dBm typ.)	< 500 mA
HSPA (Connected) Mode	Band II (1900 MHz) / V (850 MHz) for LISA-U100/U120 Band I (2100 MHz) / VIII (900 MHz) for LISA-U110/U130 5.76 Mb/s UL, 7.2 Mb/s DL Maximum Tx power (21.5 dBm typ.)	< 500 mA

Table 11: Power consumption

⁸ It is assumed that no significant load is connected to any digital and analog pin except for antenna

⁹ Maximum values for module average current consumption through the VCC pad in the listed modes/conditions, at 25°C, with VCC = 3.8 V, with a matched antenna.

¹⁰ Module is registered with the network, with a paging period of 1177 ms (2G network DRX setting = 5), with 16 neighbour cells.

¹¹ Module is registered with the network, with a paging period of 1280 ms (3G network DRX setting = 7), with 16 neighbour cells.

4.2.5 RF Performance

Parameter		Min.	Max.	Unit	Remarks
Frequency range GSM 850	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range E-GSM 900	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range DCS 1800	Uplink	1710	1785	MHz	Module transmit
	Downlink	1805	1880	MHz	Module receive
Frequency range PCS 1900	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 850 (band V)	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range UMTS 900 (band VIII)	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range UMTS 1900 (band II)	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 2100 (band I)	Uplink	1920	1980	MHz	Module transmit
	Downlink	2110	2170	MHz	Module receive

Table 12: Operating RF frequency bands

Parameter	Min.	Typ.	Max.	Unit	Remarks
Receiver input sensitivity GSM 850	-102	-110		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity E-GSM 900	-102	-110		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity DCS 1800	-102	-110		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity PCS 1900	-102	-110		dBm	Downlink RF level @ BER Class II < 2.4 %
Receiver input sensitivity UMTS 850 (band V)	-104	-112		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 900 (band VIII)	-103	-111		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 1900 (band II)	-104	-111		dBm	Downlink RF level for RMC @ BER < 0.1 %
Receiver input sensitivity UMTS 2100 (band I)	-106	-111		dBm	Downlink RF level for RMC @ BER < 0.1 %

Condition: 50 Ω source

Table 13: Receiver sensitivity performance

Parameter	Min.	Typ.	Max.	Unit	Remarks
Maximum output power GSM 850	31.0	32.5	34.0	dBm	Uplink burst RF power for Single slot TCH at maximum output power control level (PCL5)
Maximum output power E-GSM 900	31.0	32.5	34.0	dBm	Uplink burst RF power for Single slot TCH at maximum output power control level (PCL5)
Maximum output power DCS 1800	28.0	29.5	32.0	dBm	Uplink burst RF power for Single slot TCH at maximum output power control level (PCL0)
Maximum output power PCS 1900	28.0	29.5	32.0	dBm	Uplink burst RF power for Single slot TCH at maximum output power control level (PCL0)
Maximum output power UMTS 850 (Band V)	21.0	23.0	25.0	dBm	Uplink continuous RF power for RMC at maximum power (continuous UP power control command)
Maximum output power UMTS 900 (Band VIII)	21.0	22.5	25.0	dBm	Uplink continuous RF power for RMC at maximum power (continuous UP power control command)
Maximum output power UMTS 1900 (Band II)	21.0	23.0	25.0	dBm	Uplink continuous RF power for RMC at maximum power (continuous UP power control command)
Maximum output power UMTS 2100 (Band I)	21.0	23.0	25.0	dBm	Uplink continuous RF power for RMC at maximum power (continuous UP power control command)

Condition: 50 Ω output load

Table 14: Transmitter maximum output power

4.2.6 PWR_ON pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
PWR_ON	Internal supply for Power-On Input Signal	2.18	2.30	2.41	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.65	V	High input impedance (no internal pull-up)
	H-level input	2.00		4.50	V	High input impedance (no internal pull-up)
	L-level input current		-8		μ A	

Table 15: PWR_ON pin characteristics (POS domain)

4.2.7 RESET_N pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
RESET_N	Internal supply for External Reset Input Signal	2.18	2.30	2.41	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.65	V	
	H-level input	1.69		2.48	V	
	L-level input current		-230		μ A	
	Pull-up resistance		10		k Ω	Internal pull-up to RTC supply (V_BCKP)
	Minimal low time required to perform a proper reset	50			ms	

Table 16: RESET_N pin characteristics (ERS domain)

4.2.8 (U)SIM pins

The SIM pins are a dedicated interface to the (U)SIM chip card/IC. The electrical characteristics fulfill regulatory specification requirements. The values in Table 17 are for information only.

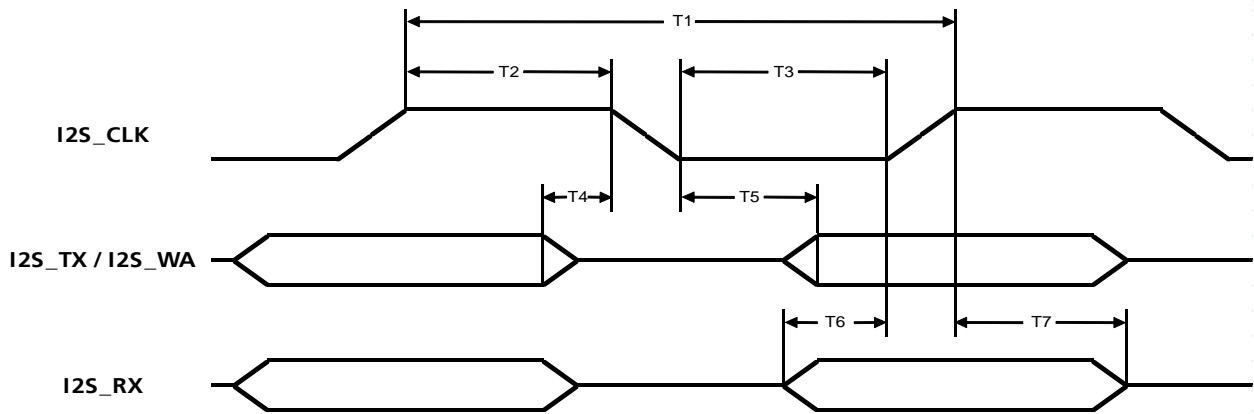
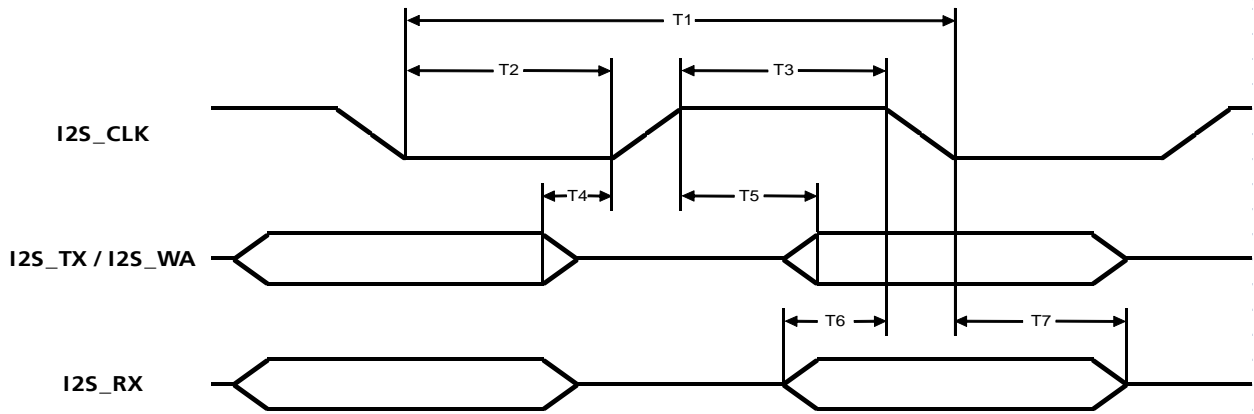
Parameter	Min.	Typ.	Max.	Unit	Remarks
Low-level input	0.00		0.36	V	VSIM = 1.80 V
	0.00		0.58	V	VSIM = 2.90 V
High-level input	1.26		3.30	V	VSIM = 1.80 V
	2.03		3.30	V	VSIM = 2.90 V
Low-level output		0.00	0.20	V	VSIM = 1.80 V, Max value at $I_{OL} = +1.0$ mA
		0.00	0.20	V	VSIM = 2.90 V, Max value at $I_{OL} = +1.0$ mA
High-level output	1.60	1.80		V	VSIM = 1.80 V, Min value at $I_{OH} = -1.0$ mA
	2.70	2.90		V	VSIM = 2.90 V, Min value at $I_{OH} = -1.0$ mA
Input/Output leakage current			0.7	μ A	$0.2V < V_{IN} < 3.3V$
Internal pull-up resistor on SIM_IO to VSIM		4.7		k Ω	
Clock frequency on SIM_CLK		3.25		MHz	

Table 17: (U)SIM pins characteristics (SIM domain)

4.2.9 Generic Digital Interfaces pins

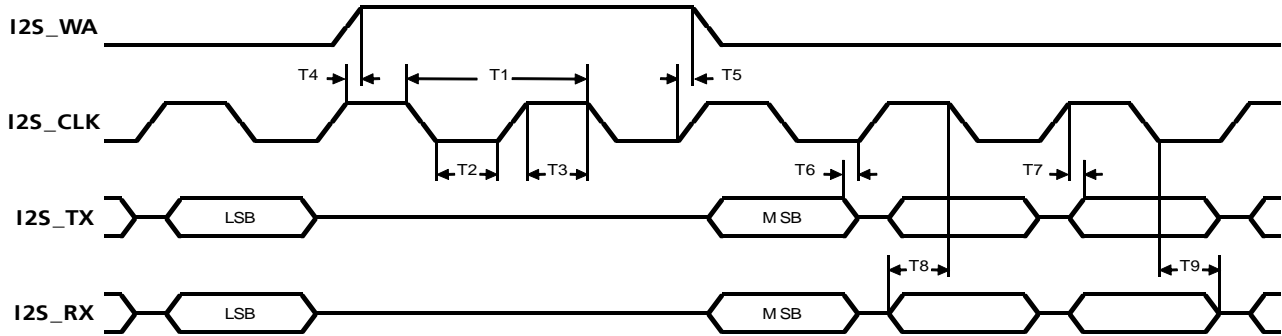
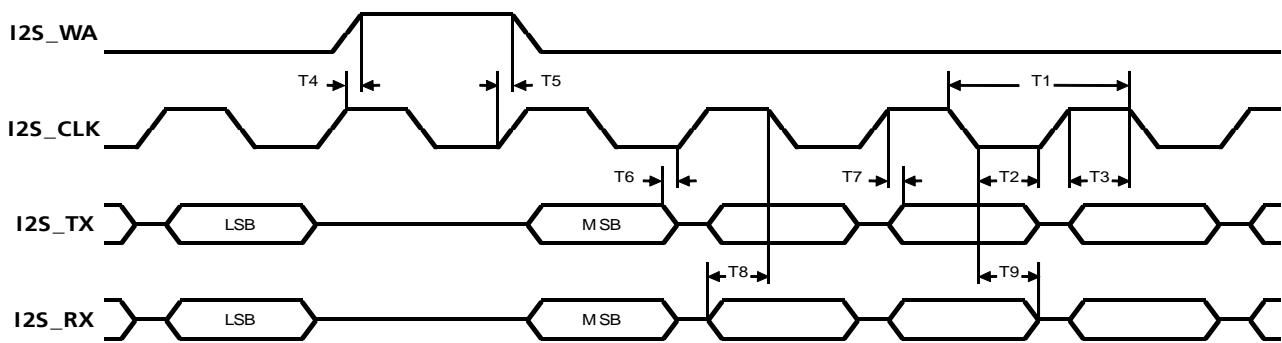
Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for GDI domain	1.77	1.80	1.83	V	Digital I/O Interfaces supply (V_INT)
Input characteristic: L-level input	-0.20		0.35	V	
Input characteristic: H-level input	1.28		1.97	V	
Output characteristics: L-level output		0.00	0.20	V	Max value at $I_{OL} = +0.1\text{mA}$ for driver class A
		0.00	0.35	V	Max value at $I_{OL} = +8.0\text{mA}$ for driver class A
		0.00	0.20	V	Max value at $I_{OL} = +0.1\text{mA}$ for driver class B
		0.00	0.35	V	Max value at $I_{OL} = +4.0\text{mA}$ for driver class B
		0.00	0.20	V	Max value at $I_{OL} = +0.1\text{mA}$ for driver class C
		0.00	0.35	V	Max value at $I_{OL} = +2.5\text{mA}$ for driver class C
		0.00	0.54	V	Max value at $I_{OL} = +1.0\text{mA}$ for driver class C_0
		0.00	0.20	V	Max value at $I_{OL} = +0.1\text{mA}$ for driver class D
Output characteristics: H-level output		0.00	0.35	V	Max value at $I_{OL} = +1.0\text{mA}$ for driver class D
	1.45	1.80		V	Min value at $I_{OH} = -8.0\text{mA}$ for driver class A
	1.60	1.80		V	Min value at $I_{OH} = -0.1\text{mA}$ for driver class A
	1.45	1.80		V	Min value at $I_{OH} = -4.0\text{mA}$ for driver class B
	1.60	1.80		V	Min value at $I_{OH} = -0.1\text{mA}$ for driver class B
	1.45	1.80		V	Min value at $I_{OH} = -2.0\text{mA}$ for driver class C
	1.60	1.80		V	Min value at $I_{OH} = -0.1\text{mA}$ for driver class C
	1.26	1.80		V	Min value at $I_{OH} = -1.0\text{mA}$ for driver class C_0
1.45	1.80		V	Min value at $I_{OH} = -1.0\text{mA}$ for driver class D	
1.60	1.80		V	Min value at $I_{OH} = -0.1\text{mA}$ for driver class D	
Input/Output leakage current			0.7	μA	$0.2\text{ V} < V_{IN} < 1.97\text{ V}$
Pull-up input current			-220	μA	PU/PD Class a
			-110	μA	PU/PD Class b
			-100	μA	PU/PD Class b_0
			-60	μA	PU/PD Class c
Pull-down input current			+200	μA	PU/PD Class a
			+100	μA	PU/PD Class b
			+85	μA	PU/PD Class b_0
			+55	μA	PU/PD Class c

Table 18: Generic Digital Interfaces pins characteristics (GDI domain)


Figure 5: AC characteristics of digital audio interface in normal I²S mode (<l2s_mode> = 2,4,6,8,10,12)

Figure 6: AC characteristics of digital audio interface in normal I²S mode (<l2s_mode> = 3,5,7,9,11,13)

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I2S_CLK period		3.906		μs	<l2s_mode> = 2,4,6,8,10,12
			3.906		μs	<l2s_mode> = 3,5,7,9,11,13
1/T1	I2S_CLK frequency		256		kHz	<l2s_mode> = 2,4,6,8,10,12
			256		kHz	<l2s_mode> = 3,5,7,9,11,13
T2	I2S_CLK high time		1.953		μs	<l2s_mode> = 2,4,6,8,10,12
			1.953		μs	<l2s_mode> = 3,5,7,9,11,13
T3	I2S_CLK low time		1.953		μs	<l2s_mode> = 2,4,6,8,10,12
			1.953		μs	<l2s_mode> = 3,5,7,9,11,13
	I2S_WA period		125.0		μs	<l2s_mode> = 2,4,6,8,10,12
			125.0		μs	<l2s_mode> = 3,5,7,9,11,13
	I2S_WA frequency		8		kHz	<l2s_mode> = 2,4,6,8,10,12
			8		kHz	<l2s_mode> = 3,5,7,9,11,13
T4	I2S_TX invalid before I2S_CLK low end			24	ns	<l2s_mode> = 2,4,6,8,10,12
	I2S_TX invalid before I2S_CLK high end			24	ns	<l2s_mode> = 3,5,7,9,11,13
T5	I2S_TX valid after I2S_CLK high begin			32	ns	<l2s_mode> = 2,4,6,8,10,12
	I2S_TX valid after I2S_CLK low begin			32	ns	<l2s_mode> = 3,5,7,9,11,13
T6	I2S_RX setup time before I2S_CLK high end	60			ns	<l2s_mode> = 2,4,6,8,10,12
	I2S_RX setup time before I2S_CLK low end	60			ns	<l2s_mode> = 3,5,7,9,11,13
T7	I2S_RX hold time after I2S_CLK low begin	10			ns	<l2s_mode> = 2,4,6,8,10,12
	I2S_RX hold time after I2S_CLK high begin	10			ns	<l2s_mode> = 3,5,7,9,11,13

Table 19: AC characteristics of digital audio interface in normal I²S mode (<l2s_mode> = 2,3,4,5,6,7,8,9,10,11,12,13)


Figure 7: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0)

Figure 8: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 1)

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I2S_CLK period		6.944		μs	<I2S_mode> = 0
			7.353		μs	<I2S_mode> = 1
1/T1	I2S_CLK frequency		144		kHz	<I2S_mode> = 0
			136		kHz	<I2S_mode> = 1
T2	I2S_CLK low time		3.472		μs	<I2S_mode> = 0
			3.676		μs	<I2S_mode> = 1
T3	I2S_CLK high time		3.472		μs	<I2S_mode> = 0
			3.676		μs	<I2S_mode> = 1
	I2S_WA period		125.0		μs	<I2S_mode> = 0
			125.0		μs	<I2S_mode> = 1
	I2S_WA frequency		8		kHz	<I2S_mode> = 0
			8		kHz	<I2S_mode> = 1
T4	I2S_CLK high begin to I2S_WA high begin	-24		32	ns	<I2S_mode> = 0
		-24		32	ns	<I2S_mode> = 1
T5	I2S_CLK low end to I2S_WA high end	-24		32	ns	<I2S_mode> = 0
		-24		32	ns	<I2S_mode> = 1
T6	I2S_TX invalid before I2S_CLK low end			24	ns	<I2S_mode> = 0
				24	ns	<I2S_mode> = 1
T7	I2S_TX valid after I2S_CLK high begin			22	ns	<I2S_mode> = 0
				22	ns	<I2S_mode> = 1
T8	I2S_RX setup time before I2S_CLK high end	60			ns	<I2S_mode> = 0
		60			ns	<I2S_mode> = 1
T9	I2S_RX hold time after I2S_CLK low begin	12			ns	<I2S_mode> = 0
		12			ns	<I2S_mode> = 1

Table 20: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0,1)

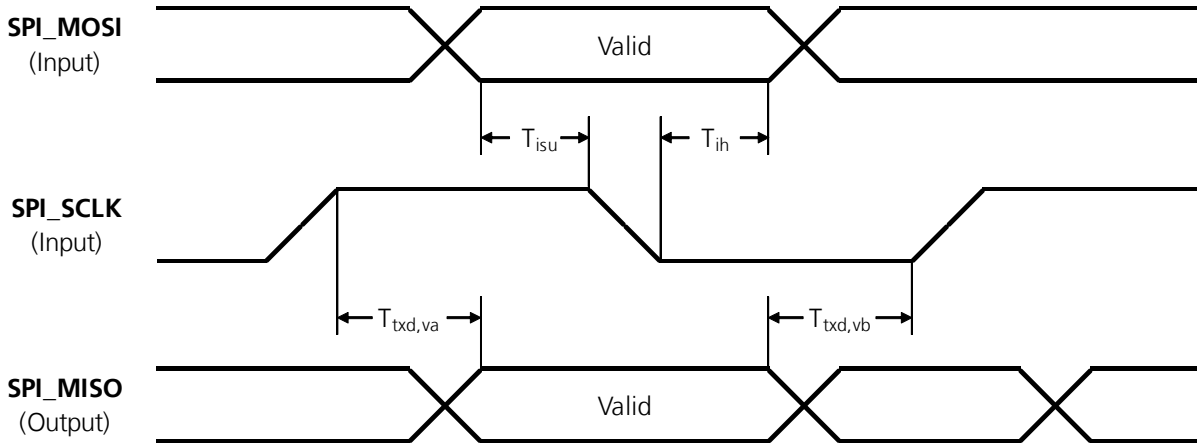


Figure 9: SPI_MOSI, SPI_MISO, SPI_SCLK timings

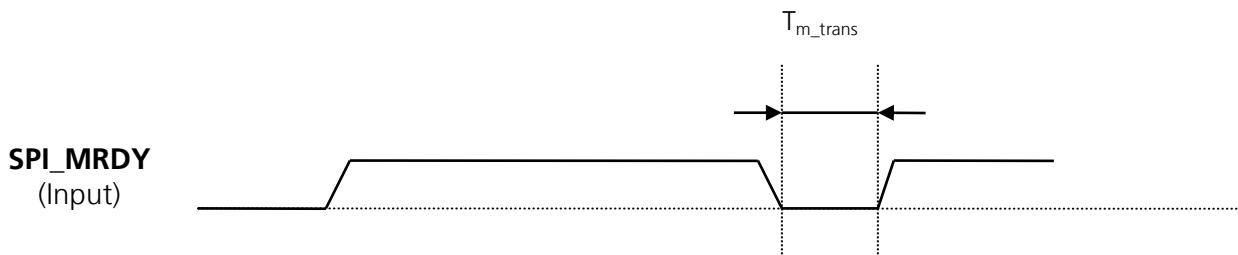


Figure 10: SPI_MRDRY transition

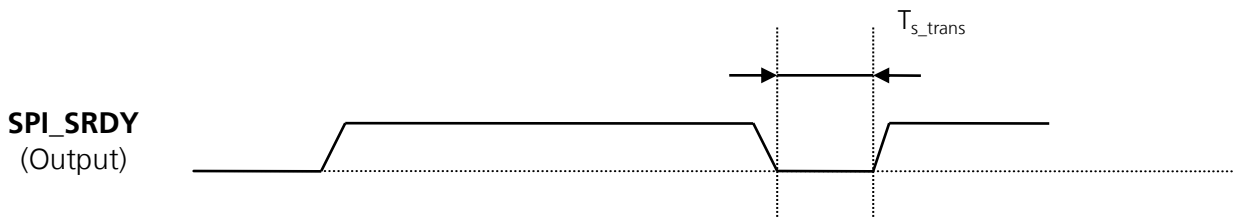


Figure 11: SPI_SRDY transition

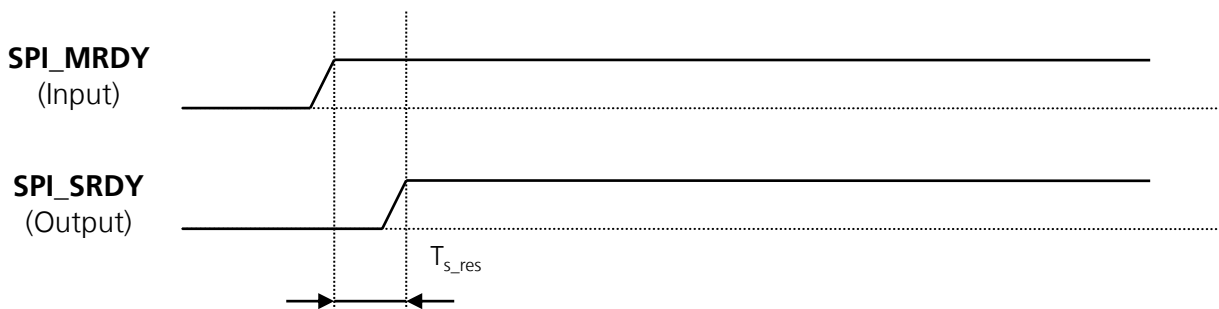


Figure 12: SPI_SRDY response

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
	SPI_SCLK frequency			26	MHz	
	SPI_SCLK period	38.5			ns	
T_{su}	Receive data setup time	5			ns	
T_{th}	Receive data hold time	5			ns	
$T_{bxd,va}$	Transmit data valid after clock rising edge			13	ns	
$T_{bxd,vb}$	Transmit data valid before clock rising edge			0	ns	
$T_{m,trans}$	Time between two master data transfers	80			ns	Power saving disabled by AT+UPSV
		62			μ s	Power saving enabled by AT+UPSV
$T_{s,trans}$	Time between two slave data transfers	80			ns	
$T_{s,res}$	SPI_SRDY active after SPI_MRDY active			200	μ s	Power saving disabled by AT+UPSV
				10	ms	Power saving enabled by AT+UPSV

Table 21: AC characteristics of SPI interface

4.2.10 USB pins

USB data lines (**USB_D+** and **USB_D-**) are compliant to the USB 2.0 high-speed specification. Refer to the Universal Serial Bus Revision 2.0 specification [10] for detailed electrical characteristics.

Parameter	Min.	Typ.	Max.	Unit	Remarks
USB detection voltage on pin VUSB_DET	4.40	5.00	5.25	V	
Current sink at VUSB_DET		150		μ A	
High-speed squelch detection threshold (input differential signal amplitude)	100		150	mV	
High speed disconnect detection threshold (input differential signal amplitude)	525		625	mV	
High-speed data signaling input common mode voltage range	-50		500	mV	
High-speed idle output level	-10		10	mV	
High-speed data signaling output high level	360		440	mV	
High-speed data signaling output low level	-10		10	mV	
Chirp J level (output differential voltage)	700		1100	mV	
Chirp K level (output differential voltage)	-900		-500	mV	

Table 22: USB pins characteristics

4.2.11 DDC (I²C) pins

DDC (I²C) lines (**SCL** and **SDA**) are compliant to the I²C-bus standard mode specification. Refer to the I²C-Bus Specification Version 2.1 [11] for detailed electrical characteristics.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for DDC domain	1.77	1.80	1.83	V	Digital I/O Interfaces supply (V_INT)
L-level input	-0.30		0.54	V	
H-level input	1.26		1.97	V	
Hysteresis	0.09			V	
L-level output		0.00	0.40	V	
Input/Output leakage current			0.7	μA	0.2 V < V _N < 1.97 V
Clock frequency on SCL		100		kHz	

Table 23: DDC (I²C) pins characteristics (DDC domain)

4.2.12 Audio pins

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
MIC_P/MIC_N	Differential input voltage			0.8	Vpp	Full scale differential voltage
	Differential input resistance		50		kΩ	
	Input capacitance		100		nF	Internal DC blocking capacitor at MIC_P and MIC_N pins
	Signal to noise	75			dB	Gain stage = +12 dB, Bandwidth 300-3900 Hz
	Signal to distortion (THD)	65			dB	
	Power supply rejection	45	66		dB	

If not specified otherwise, all parameters are measured with a bandwidth of 20 Hz,..., 20 kHz.

Table 24: Differential audio transmit path (MIC_P, MIC_N) input characteristics

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
SPK_P/SPK_N	Maximum differential output voltage	3.3	3.7	4.1	Vpp	Full scale differential open circuit voltage
	Common mode output voltage		1.25		V	
	Output load resistance	14			Ω	
	Single-ended output load capacitance			250	pF	
	Signal to noise	76	80		dB	Load = 16 Ω, Gain stage = +0 dB, Input signal = 0 dBFS, Code 0, A-weighted
	Signal to distortion (THD)	60	70		dB	Load = 16 Ω, Input signal = 0 dBFS

If not specified otherwise, all parameters are measured with a bandwidth of 20 Hz,..., 20 kHz.

Table 25: Differential audio receive path (SPK_P, SPK_N) output characteristics

5 Mechanical specifications

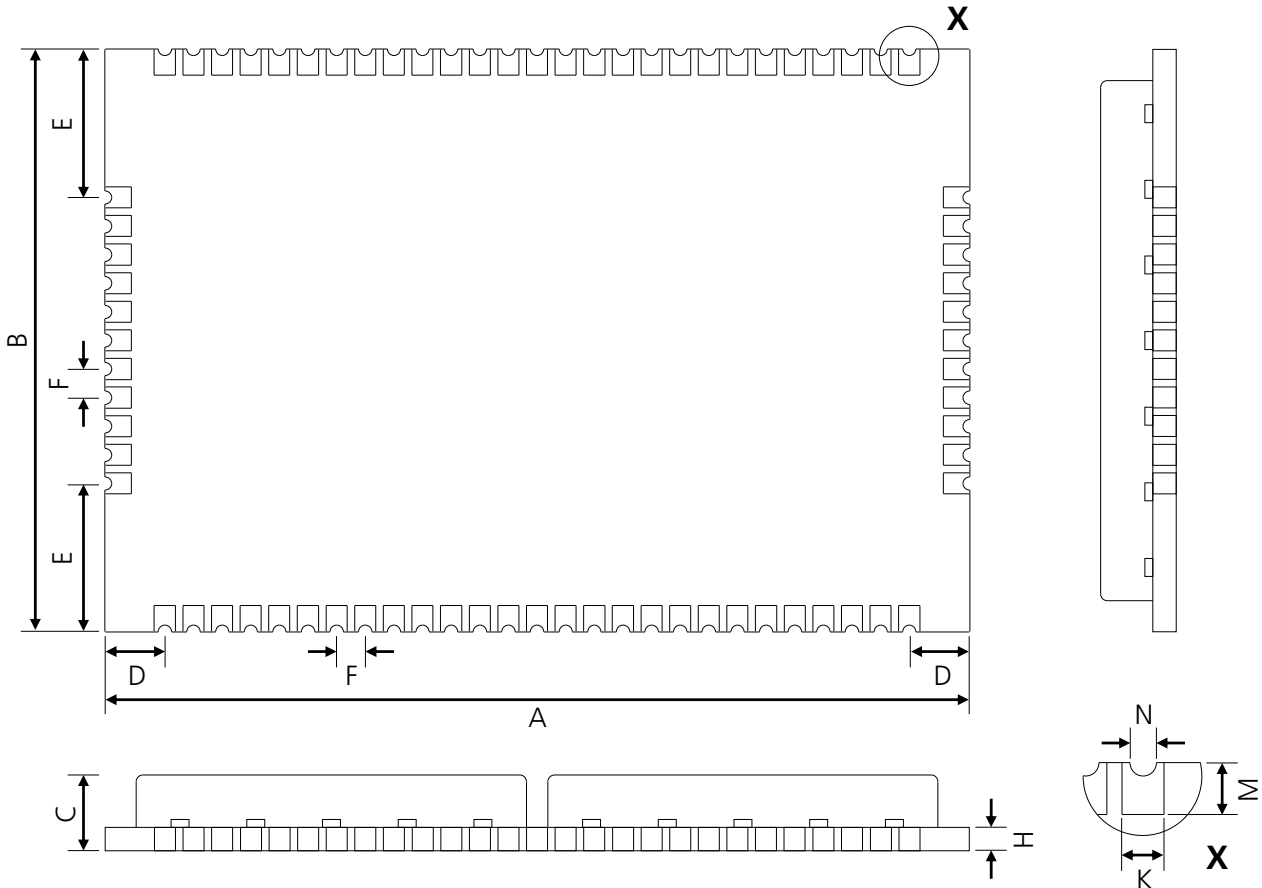


Figure 13: Dimensions (LISA-U1 series bottom and sides views)

Parameter	Description	Min.		Typ.		Max.	
A	Height (mm)	33.1	[1303.1 mil]	33.2	[1307.1 mil]	33.5	[1316.9 mil]
B	Width (mm)	22.3	[878.0 mil]	22.4	[881.9 mil]	22.5	[885.8 mil]
C	Total Thickness (mm)	TBD		2.7	[106.3 mil]	TBD	
D	Horizontal Edge to Pin Pitch (mm)	5.6	[220.5 mil]	5.7	[224.4 mil]	5.8	[228.3 mil]
E	Vertical Edge to Pin Pitch (mm)	2.2	[86.6 mil]	2.3	[90.6 mil]	2.4	[94.5 mil]
F	Pin to Pin Pitch (mm)	1.0	[39.4 mil]	1.1	[43.3 mil]	1.2	[47.2 mil]
K	Pad width (mm)	0.7	[2.8 mil]	0.8	[3.1 mil]	0.9	[3.5 mil]
M	Pad height (mm)	0.9	[3.5 mil]	1.0	[3.9 mil]	1.1	[4.3 mil]
N	Pad half-moon diameter (mm)	0.4	[1.6 mil]	0.5	[2.0 mil]	0.6	[2.4 mil]
Weight	(g)			< 8			

Note: values in mil in square brackets has been calculated from the measure in mm. Approximation to first decimal value has been applied

Table 26: Dimensions



For information regarding Footprint and Paste Mask see the LISA-U1 series System Integration Manual [6].

6 Reliability tests and approvals

6.1 Reliability tests

Qualifications according to ISO 16750 "Road vehicles - Environmental conditions and testing for electrical and electronic equipment".

6.2 Approvals



Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

LISA-U1 series modules are RoHS compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

LISA-U1 series modules are or will be approved under the schemes reported in Table 27.

Country	Scope	LISA-U100	LISA-U110	LISA-U120	LISA-U130
EU	R&TTE	YES	YES	YES	YES
EU	CE (NB ID: 0890)	YES	YES	YES	YES
US	FCC	XPYLISAU120	XPYLISAU120	XPYLISAU120	XPYLISAU120
US	PTCRB	YES	YES	YES	YES
EU	GCF – CC	YES	YES	YES	YES
Canada	Industry Canada (IC)	8595A-LISAU120	8595A-LISAU130	8595A-LISAU120	8595A-LISAU130

Table 27: LISA-U1 series certification approvals

For more details on all country certification and network operators please refer to our website www.u-blox.com.

7 Product handling

7.1 Packaging

LISA-U1 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down.



Figure 14: Reeled LISA-U1 series modules

7.1.1 Reels

LISA-U1 series modules are deliverable in quantities of 150 pieces on a reel. The dimension of the reel is shown in Figure 15.



Quantities of less than 150 pieces are also available. Contact u-blox for more information.

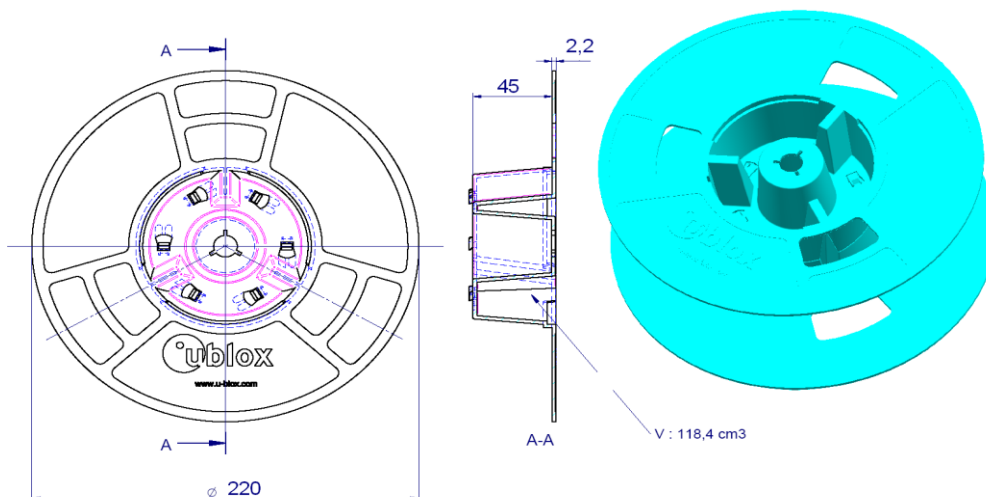


Figure 15: Dimensions of reel (measurements are in mm, unless otherwise specified)

7.1.2 Tapes

The dimensions and orientations of the tapes for LISA-U1 series modules are specified in Figure 16.

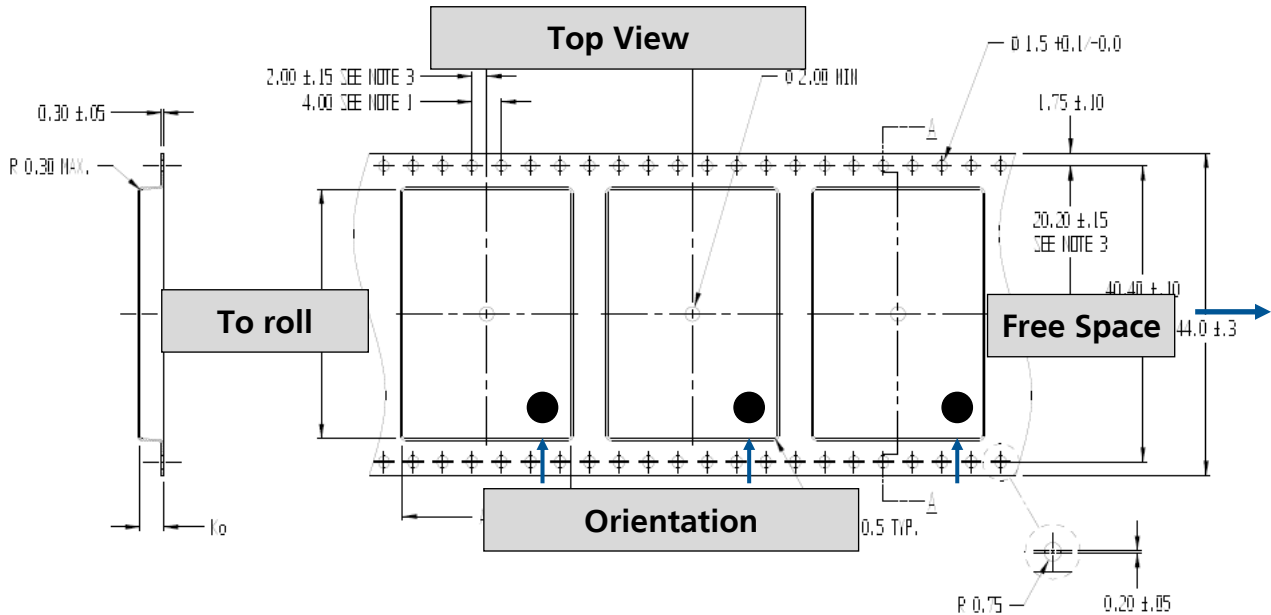


Figure 16: Dimensions for LISA-U1 series on tape

7.2 Shipment, storage and handling

LISA-U1 series modules are designed and packaged to be processed in an automatic assembly line, and are shipped in Tape-and-Reel.

- ⚠ **LISA-U1 series modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification. Appropriate MSD handling instructions and precautions are summarized in Sections 7.2.1 to 7.2.4. Read them carefully to prevent permanent damage due to moisture intake.**
- ⚠ **LISA-U1 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling LISA-U1 series modules without proper ESD protection may destroy or damage them permanently. See Section 7.1 for ESD handling instructions.**

7.2.1 Moisture sensitivity levels

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. LISA-U1 series modules are rated at MSL level 4.

- 👉 For MSL standard see IPC/JEDEC J-STD-020 (can be downloaded from www.jedec.org).

7.2.2 Shipment

Table 28 summarizes the dry pack requirements for different MSL levels in the IPC/JEDEC specification.

MSL Level	Dry Pack Requirement
1	Optional
2	Required
2a	Required
3	Required
4	Required

Table 28: JEDEC specification of dry pack requirements

According to IPC/JEDEC specification J-STD-020, if a device passes MSL level 1, it is classified as not moisture sensitive and does not require dry pack. If a device fails level 1 but passes a higher numerical level, it is classified as moisture sensitive and must be dry packed in accordance with J-STD-033.

LISA-U1 series modules are delivered on Tape-and-Reels in a hermetically sealed package (“dry bag”) to prevent moisture intake and protect against electrostatic discharge. For protection from physical damage, the reels are individually packed in cartons.

Carrier materials such as trays, tubes, reels, etc., that are placed in the Moisture Barrier Bag (MBB) can affect the moisture level within the MBB. Therefore, the effect of these materials is compensated by adding additional desiccant in the MBB to ensure the shelf life of the SMD packages.

The dry bag provides an IPC/JEDEC compliant MSD label describing the handling requirements to prevent humidity intake. IPC/JEDEC specifications require that MSD sensitive devices be packaged together with a Humidity Indicator Card (HIC) and desiccant to absorb humidity. If no moisture has been absorbed, the three fields in the HIC indicate blue color. Figure 17 shows examples of an MSD label and HIC.

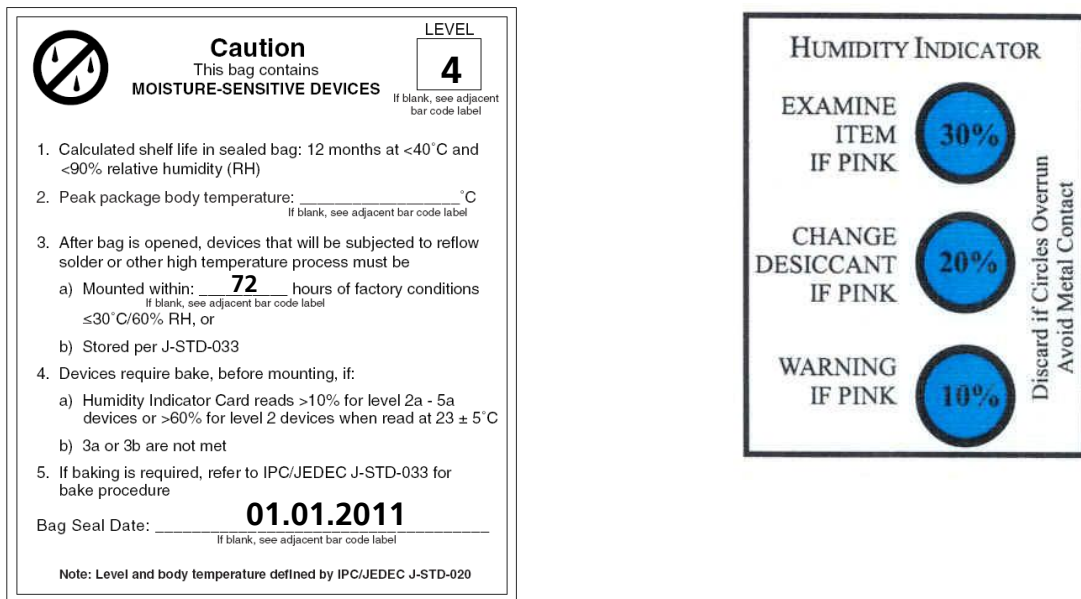


Figure 17: Examples of MSD Label and Humidity Indicator Card

7.2.3 Storage and floor life

The calculated shelf life for dry packed SMD packages is a minimum of 12 months from the bag seal date, when stored in a non-condensing atmospheric environment of <40°C/90% RH.

Table 29 lists floor life for different MSL levels in the IPC/JEDEC specification.

MSL Level	Floor life (out of bag) at factory ambient $\leq 30^{\circ}\text{C}/60\% \text{ RH}$ or as stated
1	Unlimited at $\leq 30^{\circ}\text{C}/85\% \text{ RH}$
2	1 year
2a	4 weeks
3	168 hours
4	72 hours

Table 29: JEDEC specification of floor life


The parts must be processed and soldered within the time specified for the MSL level. If this time is exceeded, or the humidity indicator card in the sealed package indicates that they have been exposed to moisture, the devices need to be pre-baked before the reflow solder process (see Section 7.2.4).


7.2.4 Drying

Both encapsulant and substrate materials absorb moisture. IPC/JEDEC specification J-STD-020 must be observed to prevent cracking and delamination associated with the “popcorn” effect during reflow soldering. The popcorn effect can be described as miniature explosions of evaporating moisture. Baking before processing is required in the following cases:

- Humidity indicator card: At least one circular indicator is no longer blue
- Floor life or environmental requirements after opening the seal have been exceeded, e.g. exposure to excessive seasonal humidity.

Refer to Section 4 of IPC/JEDEC J-STD-033 for recommended baking procedures. Table 4-1 of the specification lists the required bake times and conditions for drying. For example, a LISA-U1 series module that has exceeded its floor life by >72 hours shall be baked at 125°C for 9 hours. (Floor life begins counting at time = 0 after bake).

 **Do not attempt to bake LISA-U1 series modules while contained in tape and rolled up in reels. For baking, place parts individually onto oven tray.**

 **Oxidation risk: Baking SMD packages may cause oxidation and/or intermetallic growth of the terminations, which if excessive can result in soldering problems during board assembly. The temperature and time for baking SMD packages are therefore limited by solderability considerations. The cumulative bake time at a temperature greater than 90°C and up to 125°C shall not exceed 96 hours. If the bake temperature is not greater than 90°C , there is no limit on bake time. Bake temperatures higher than 125°C are not allowed.**

7.2.5 Reflow soldering

Reflow profiles are to be selected according to IPC/JEDEC J-STD-020.

7.2.6 ESD precautions

LISA-U1 series modules are Electrostatic Sensitive Devices (ESD) and require special ESD precautions typically applied to ESD sensitive components.

Maximum ESD ratings of the LISA-U1 series module are reported in Table 6.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates LISA-U1 series module.

ESD precautions should be implemented on the application board where the module is mounted, as described in the LISA-U1 series System Integration Manual [6].

 **Failure to observe these precautions can result in severe damage to the device!**

8 Default settings

Interface	AT Settings	Comments
UART interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: <ul style="list-style-type: none"> Channel 0: control channel Channel 1 – 5: AT commands /data connection Channel 6: GPS tunneling
	AT+IPR=115200	Baud rate: 115200 b/s
	AT+ICF=0,0	Frame format: 8 bits, no parity, 1 stop bit
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
USB interface	Enabled	6 CDCs are available, configured as described in the following list: <ul style="list-style-type: none"> USB1: AT commands / data connection USB2: AT commands / data connection USB3: AT commands / data connection USB4: GPS tunneling dedicated port USB5: 2G trace dedicated port USB6: 3G trace dedicated port
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
SPI interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: <ul style="list-style-type: none"> Channel 0: control channel Channel 1 – 5: AT commands /data connection Channel 6: GPS tunneling
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
Power Saving	AT+UPSV=0	Disabled
Network registration	AT+COPS=0	Self network registration

Table 30: Default settings

Refer to the u-blox AT Commands Manual [5] and to the LISA-U1 series System Integration Manual [6] for information about further settings.

9 Labeling and ordering information

9.1 Product labeling

The label on u-blox modules includes important product information. The location of the product type number is shown in Figure 18.

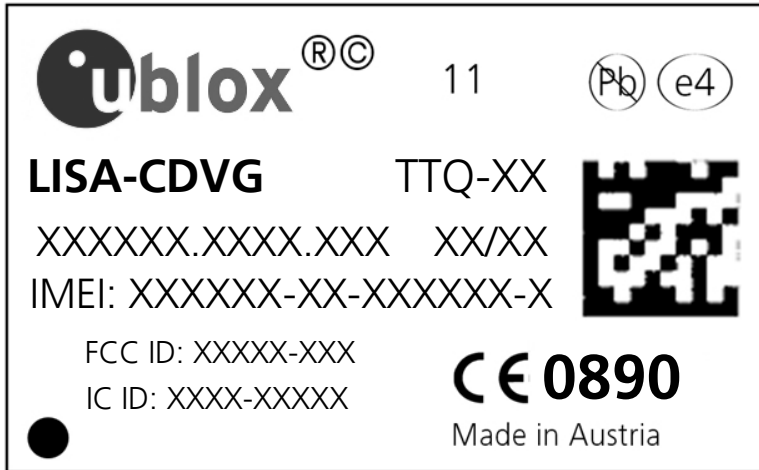


Figure 18: Location of product type number on LISA-U1 series module label

9.2 IMEI

TAC (Type Allocation Code): The TAC (Type Allocation Code) number is represented by the first 8 digits of IMEI. For LISA-U1 series the value are reported below:

- LISA-U100: 35530704
- LISA-U110: 35530504
- LISA-U120: 35530604
- LISA-U130: 35530404

9.3 Explanation of codes

3 different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 31 details these 3 different formats:

Format	Structure
Product Name	LISA-CDVG
Ordering Code	LISA-CDVG-TTQ
Type Number	LISA-CDVG-TTQ-XX

Table 31: Product Code Formats

The parts of the product code are explained in Table 32.

Code	Meaning	Example
C	Cellular standard (i.e. G: GSM; E: EDGE; W: WEDGE; H: HSDPA; U: HSUPA, P: HSPA+; L: LTE; C: CDMA)	U: HSUPA
D	Generation, e.g. chip or function set; range[0...9]	2
V	Variant based on the same cellular chip range: [0...9]	
G	GPS generation (if GPS functionality available)	6 = u-blox 6, 0: no GPS functionality
TT	Major product version	0
Q	Quality grade/production site <ul style="list-style-type: none"> • S = standard / made in Austria • A = automotive / made in Austria • B = standard / made in Brazil 	S
XX	Minor product version (not relevant for certification)	Default value is 00

Table 32: Part identification code

9.4 Ordering information

Ordering No.	Product
LISA-U100-00S	HSPA 850/1900 MHz, quad-band GPRS/EDGE, data only (no voice), 33.2 x 22.4 x 2.7 mm, 150 pcs/reel
LISA-U110-00S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, data only (no voice), 33.2 x 22.4 x 2.7 mm, 150 pcs/reel
LISA-U120-00S	HSPA 850/1900 MHz, quad-band GPRS/EDGE, voice and data, 33.2 x 22.4 x 2.7 mm, 150 pcs/reel
LISA-U130-00S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, voice and data, 33.2 x 22.4 x 2.7 mm, 150 pcs/reel

Table 33: Product ordering codes

Appendix

A Glossary

Name	Definition
AUDIO	Audio Pins (power domain)
DDC	DDC Interface (power domain)
Driver Class	Output Driver Class: see Table 18 for definition
ERS	External Reset Signal (power domain)
ESD	Electrostatic Discharge
GDI	Generic Digital Interfaces (power domain)
H	High
HBM	Human Body Model
I	Input (means that this is an input port for LISA)
L	Low
LCC	Leadless Chip Carrier
N/A	Not Applicable (used in the I/O field of pinout)
NC	Do not connect
O	Output (means that this is an output port of LISA)
PD	Pull-Down
POS	Power-On Input (power domain)
PU	Pull-Up
PU/PD Class	Pull Class: see Table 18 for definition
SIM	SIM Interface (power domain)
T	Tristate
TBF	Temporary Block Flow
USB	Universal Serial Bus (power domain)

Table 34: Explanation of abbreviations and terms used

Related documents

- [1] 3GPP TS 27.007 V3.13.0 - AT command set for User Equipment (UE) (Release 1999)
- [2] 3GPP TS 27.005 V3.2.0 (2002-06) - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS) (Release 1999)
- [3] 3GPP TS 27.010 V3.4.0 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol (Release 1999)
- [4] ITU-T Recommendation V24, 02-2000. List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Connection Equipment (DCE)
- [5] u-blox AT Commands Manual, Docu No WLS-SW-11000
- [6] LISA-U1 series System Integration Manual, Docu No 3G.G2.HW.10002
- [7] GPS Implementation Application Note, Docu No GSM.G1-CS-09007
- [8] GSM MUX Implementation Application Note for wireless modules, Docu No WLS-CS-11002
- [9] 3GPP TS 26.267 - Technical Specification Group Services and System Aspects; eCall Data Transfer; In-band modem solution; General description (Release 9)
- [10] Universal Serial Bus Revision 2.0 specification, <http://www.usb.org/developers/docs/>
- [11] I2C-Bus Specification Version 2.1 Philips Semiconductors (January 2000), http://www.nxp.com/acrobat_download/literature/9398/39340011_21.pdf
- [12] u-blox SPI Interface Application Note, Docu No 3G.G2-CS-11000



For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

Revision history

Revision	Date	Name	Status / Comments
-	24/09/2010	mbud / gcap / lpah	Initial release
1	11/10/2010	lpah	Improvements in the pinout table and dimensions figure
2	03/12/2010	sses	Some improvements inserted
3	22/04/2011	lpah	Updated status to Advance Information
4	05/07/2011	lpah	Updated status to Preliminary
5	03/08/2011	lpah	Minor improvements

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